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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/874,163	06/05/2001	Chung-Che Wu	JCLA7083	5881

7590 10/17/2003

J.C. PATENTS INC.
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IRVINE, CA 92618

EXAMINER	
KIM, HONG CHONG	

ART UNIT	PAPER NUMBER
2186	4

DATE MAILED: 10/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/874,163	Applicant(s) WU ET AL.	
	Examiner Hong C Kim	Art Unit 2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 June 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

1 dr

Detailed Action

1. Claims 1-13 are presented for examination. This office action is in response to the application filed on 6/5/01.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

3. Applicants are reminded of the duty to disclose information under 37 CFR 1.56.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

5. Claims 1, and 4-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Chang et al. (Chang) U.S. Patent No. 6,498,759.

As to claim 1, Chang discloses the invention as claimed. Chang discloses a method of automatically determining a type of a memory applied in a computer system (Fig. 5), wherein the computer system comprises a system power state signal (Fig. 5 Ref. S51), a voltage control circuit and at least one memory module slot to accommodate a memory(Fig. 5 Ref. S52), the method comprising: outputting a preset voltage to the memory(Fig. 5 Ref. S 52); performing an operation on the memory (Fig. 5 Ref. 53); determining a type of the memory (Fig. 5 Ref. 54); outputting a control signal (Fig. 5 Refs. 54-56); outputting a voltage adjustment signal according to the control signal and the system power state signal (Fig. 5 Refs. 54-56); and outputting a configured operation voltage to the memory according to the voltage adjustment signal (Fig. 5 Refs. 54-56).

As to claim 4, Chang further discloses a processor executes a software program to perform the operation on the memory, to determine the type of the memory, and to output the control signal (Fig. 5 Refs. 53-56).

As to claim 5, Chang further discloses performing the operation on the memory with the software program, which software program then determines the type of the memory when the computer system enters a reset state (Fig. 5 Refs. 53-56).

As to claim 6, Chang further discloses a hardware device performs the operation on the memory, determines the type of the memory, and outputs the control signal (Fig. 5 Refs. 53-56).

As to claim 7, Chang further discloses the operation comprises an access operation (Fig. 5).

As to claim 8, Chang discloses the invention as claimed. Chang discloses a motherboard (Fig. 1 Ref. 100) to automatically determine a type of a memory, used in a computer system that has a system power state signal, the motherboard comprising: a hardware device (Fig. 1), generating a control signal (Fig 1); a memory module slot, accommodating a memory (Fig. 1 Ref. 130); a voltage control circuit (Fig. 1 Ref. 140), coupled to the memory module slot to provide a configured operation voltage to the memory module slot (Fig. 5 Refs 54-56); and a recognition apparatus, coupled to the system power state signal (Fig. 1), the control signal and the voltage control circuit (Fig. 1); wherein the voltage control circuit firstly outputs a preset voltage to the memory (Fig. 5 Ref. 52) and then the hardware device outputs the control signal after performing an operation to determine a type of the memory (Fig. 5 Refs. 51-54); and the recognition apparatus outputs a voltage adjustment signal after receiving the control signal (Fig. 5 Refs. 54-56) and the system power state signal, so that the voltage control circuit outputs the configured operation voltage to the memory (Fig. 5 Refs. 54-56).

As to claim 9, Chang further discloses the hardware device comprises a central process unit executing a software program to generate the control signal (Fig. 3 Ref. 305).

As to claim 10, Chang further discloses the voltage adjustment signal is configured as a high logic state when the system power state signal is a low logic state; the voltage adjustment signal is configured as a low logic state when the control signal to be converted from the low logic state to the high logic state and the system power state signal is the high logic state; and the voltage adjustment signal otherwise remains a previous logic state (Fig. 2).

As to claim 11, Chang further discloses the recognition apparatus further comprises: an inverter, having an input terminal and an output terminal, wherein the input terminal is coupled to the control signal; and a D-flip-flop, comprising a data terminal, a clock terminal, a clear terminal, an inverted output terminal and a preset terminal, wherein the data terminal is coupled to the output terminal of the inverter, the clock terminal is coupled to the control signal, the clear terminal is coupled to the system power state signal, the inverted output terminal is coupled to the voltage adjustment signal, and the preset terminal is coupled to a specific voltage; wherein when the clear terminal is the low logic state, the inverted output terminal is configured to the high logic state, when the clear terminal is the high logic state and the clock terminal is converted from the low logic state to the high logic state the inverted output terminal is configured to the

low logic state, and the inverted output terminal is otherwise maintained at the previous logic state (Fig. 2).

As to claim 12, Chang further discloses the D-flip-flop comprises an RS D-flip-flop (Fig. 2).

As to claim 13, Chang further discloses the operation comprises an access operation (Fig. 5 Refs. 53-56).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. (Chang) U.S. Patent No. 6,498,759 as applied to claim 1 above, and further in view of Applicant's Admitted Prior Art (AAPA) page2.

As to claims 2-3, Chang discloses the claimed invention, however, Chang does not specifically disclose STD and STR modes. AAPA discloses STD and STR modes (page 2 lines

6-11) for the purpose of providing power saving modes thereby consuming less power and generating less heat in the system.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate STD and STR modes as shown in AAPA into the invention of Chang because it would provide power saving modes thereby consuming less power and generating less heat in the system.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See attached PTO-892.

9. a shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

10. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. § 1.111(c).

11. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

12. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Hong Kim whose telephone number is (703) 305-3835. The Examiner can normally be reached on the weekdays from 8:30 AM to 5:00 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Matt Kim, can be reached on (703) 305-3821.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

13. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to TC-2100:
After-Final (703) 746-7238
Official (703) 746-7239 (for formal communications intended for entry)

Non-Official/Draft (703) 746-7240 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

HK
Primary Patent Examiner
October 5, 2003